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TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-2047

In re Application of: Akihiko Koh et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/802,857-Conf. #3304	March 12, 2001	M. J. Yigdall	2192

Invention: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: April 24, 2008 .

The fee for filing this Appeal Brief is $ 510.00 .

[X] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

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This sheet is submitted in duplicate.

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[X] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 18-0013 .
This sheet is submitted in duplicate.

45,290

Dated: June 25, 2008

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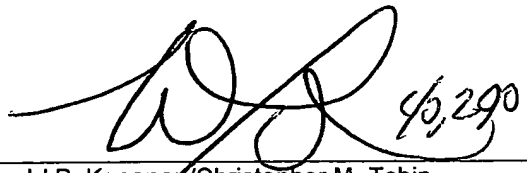

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Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Application No.: 09/802,857 | Confirmation No.: 3304

Filed: March 12, 2001 | Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM | Examiner: M. J. Yigdall

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated December 28, 2007. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately. This brief is in furtherance of the Final Office Action on December 28, 2007.

A Notice of Appeal was filed in this case on April 24, 2008, along with a Request for Panel Review.

The Notice of Panel Decision from Pre-Appeal Brief Review mailed on May 27, 2008. ("the Decision") indicates that claims 27-28, 40 and 45-52 remain rejected.

The Decision further indicates that the extendable time period for the filing of the Appellant's Brief will be reset to be one month from the mailing of the Decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater.

Accordingly, the filing of the Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 011655, frame 0005.**

II. RELATED APPEALS AND INTERFERENCES

Within the Decision on Appeal mailed October 31, 2006, the Board of Patent Appeals and Interferences (the Board) concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of prior claims 13-25 under 35 U.S.C. §103.

Within the Decision on Rehearing mailed on June 21, 2007, the Board has maintained its earlier conclusion rendered in the Decision on Appeal of October 31, 2006 regarding claims 13-25.

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 27-28, 40 and 45-52 are currently pending in this application, with claims 27, 40 and 45 being independent.

Within the Final Office Action of December 28, 2007:

Paragraph 6 of the Office Action indicates a rejection of claims 45-52 under 35 U.S.C. §112, second paragraph.

Paragraph 8 of the Office Action indicates a rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).

Paragraph 9 of the Office Action indicates a rejection of claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).

Paragraph 10 of the Office Action indicates a rejection of claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

Thus, the status of the claims is as follows:

Claims 1-26. (Canceled);

Claims 27-28. (Rejected);

Claims 29-39. (Canceled);

Claim 40. (Rejected);

Claims 41-44. (Canceled);

Claims 45-52. (Rejected).

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 27-28, 40 and 45-52 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of December 28, 2007, an Amendment After Final Office Action Under 37 C.F.R. 1.116 has been filed on February 15, 2008.

The Advisory Action of April 9, 2008 denied entry of the Amendment.

No other Amendments have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 27. A data processing apparatus comprising:	Paragraphs within U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application.
a bug address setting register (110, 110-1, 110-2) adapted to store a bug address, said bug address indicating an address for a buggy data;	Paragraph [0054]
a coincidence detecting circuit (120, 120-1, 120-2) adapted to compare said address with said bug address and output an interrupt request signal, said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address;	Paragraphs [0054], [0055], [0072]
a central processing unit (10) adapted to process an interrupt function upon receipt of said interrupt request signal; and	Paragraph [0062]
a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.	Paragraph [0075]

Claim 40 is drawn to a data processing apparatus comprising:	Paragraphs within U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application.
program memory (30) adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;	Paragraphs [0050], [0051]
a bug address setting register (110, 110-1, 110-2) adapted to store a bug address, said bug address indicating a starting address within said program memory (30) for a buggy part of said program; and	Paragraph [0054]
a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address,	Paragraph [0075]
wherein another program address indicates a location within said program memory (30) for another of the instruction codes, and	Paragraph [0066]
wherein said value of the counter register is incremented by 1.	Paragraph [0075]

Claim 45 is drawn to a data processing apparatus comprising:	Paragraphs within U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application.
program memory (30) adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;	Paragraphs [0050], [0051]
a central processing unit (10) adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal (S_{A1}) or a second interrupt request signal (S_{A2});	Paragraph [0054]
a first coincidence detecting circuit (120-1) adapted to compare said program address with a first bug address and output said first interrupt request signal (S_{A1}), said central processing unit (10) receiving said first interrupt request signal (S_{A1});	Paragraph [0075]
a second coincidence detecting circuit (120-2) adapted to compare said program address with a second bug address and output said second interrupt request signal (S_{A2}), said central processing unit (10) receiving said second interrupt request signal (S_{A2});	Paragraph [0066]
a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,	Paragraph [0075]
wherein said counter register is set to 0 during said initialization processing.	Paragraph [0075]

Claim 52 is drawn to a data processing apparatus as set forth in claim 51,	Paragraphs within U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application.
wherein said first and second interrupt request signals are AND'ed together to become said single interruption.	Paragraphs [0073], [0074]

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 45-52 under 35 U.S.C. §112, second paragraph.

Whether the Examiner erred in rejecting claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).

Whether the Examiner erred in rejecting claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).

Whether the Examiner erred in rejecting claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

These issues will be discussed hereinbelow.

VII. ARGUMENT

In the Final Office Action of December 28, 2007:

> The Examiner erred in rejecting claims 45-52 under 35 U.S.C. §112, second paragraph.
>
> The Examiner erred in rejecting claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).
>
> The Examiner erred in rejecting claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).
>
> The Examiner erred in rejecting claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

For at least the following reasons, Appellant submits that these rejections are both technically and legally unsound and should therefore be reversed.

1. **The Examiner erred in rejecting claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki).**

This rejection is traversed at least for the following reasons.

Claims 27-28 stand or fall together - Claim 28 is dependent upon claim 27. Claim 27 is drawn to a data processing apparatus comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data;

a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal, said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address;

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Sagane and Suzuki, either individually or as a whole, fail to disclose, teach, or suggest a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data.

Claims 40 stands or falls alone - Claim 40 is drawn to a data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address,

wherein another program address indicates a location within said program memory for another of the instruction codes, and

wherein said value of the counter register is incremented by 1.

Sagane - Sagane ***fails*** to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein said value of the counter register is incremented by 1.

Suzuki - The Office Action cites Suzuki for the features that are deficient from within Sagane.

As shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the residual 2 bits (MSB and bit 6) are set to express the *number of correcting portions* in the module, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)) (Suzuki at column 4, lines 41-45).

As a rule, the teachings, suggestions or incentives supporting the obviousness-type rejection must be clear and particular. Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

However, Suzuki ***fails*** to disclose, teach, or suggest that number of correcting portions is *incremented by 1*. Instead, Suzuki merely teaches that the stored number of correcting portions S is ***decremented*** (step S28) (Suzuki at column 6, lines 61-62). The Office Action ***fails*** to provide any objective evidence sufficient to show that decrementing and incrementing the number of correcting portions are one in the same.

To account for these deficiencies within Suzuki, the Office Action concludes, *without providing any supporting evidence*, that a person of ordinary skill in the art at the time the invention

was made *could* implement the counter register such that the value is incremented by 1 *rather than* decremented by 1 with predictable results (Office Action at page 12).

Assertions of technical facts in areas of esoteric technology ***must always be supported by citation to some reference work*** recognized as standard in the pertinent art. *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

Here, the Office Action ***fails*** to show where within Suzuki there is taught that *a specific amount* by which the stored number of correcting portions S is decremented, or that the stored number of correcting portions S is *decremented by 1*.

Moreover, the Office Action ***fails*** to show where within Suzuki there is taught that the stored number of correcting portions S *is* ***INCREMENTED*** or that the stored number of correcting portions S ***is INCREMENTED by 1***.

Nevertheless, the Office Action asserts that it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value of the counter register is ***incremented by 1*** (Office Action at page 12).

In response, incrementing is ***absent*** from within Suzuki. Instead, Suzuki arguably teaches that as a result of the ***decrement***, it is checked whether or not the number of correcting portions is 0 (Suzuki at column 6, lines 62-64).

The Office Action urges that one ***could*** implement Suzuki such that the value is initialized to 0 and step S29 (FIG. 4B) checks for whether the value is equal to the number stored in step S5 (FIG. 4A), *rather than checking for whether the value is equal to 0* (Office Action at page 12).

In response, such a retrospective view *is not a substitute* for some objective teaching or suggestion supporting an obviousness rejection since the assertions and urgings presented within the Office Action amount to nothing more than an "obvious-to-try" situation.

Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990).

Moreover, an invention is "obvious-to-try" where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful. *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, the cited prior art does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious-to-try" is not the standard under §103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

- ***Thus, Sagane and Suzuki, either individually or as a whole, fail to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein said value of the counter register is incremented by 1.***

Withdrawal of this rejection and allowance of the claims is respectfully requested.

2. **The Examiner erred in rejecting claims 45-52 under 35 U.S.C. §112, second paragraph; and**

3. **The Examiner erred in rejecting claims 45-50 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki); and**

4. **The Examiner erred in rejecting claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).**

These rejections are traversed at least for the following reasons.

Regarding the rejection 35 U.S.C. §112, second paragraph, as an initial matter, while not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, an amendment to claim 45 in the manner suggested by the Examiner has been proposed amended within the Amendment After Final Office Action Under 37 C.F.R. 1.116 of February 15, 2008.

Claims 45-51 stand or fall together - Claims 46-51 are dependent upon 45. Claim 45 is drawn to a data processing apparatus comprising:

> program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;
>
> a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

Sagane and Suzuki, either individually or as a whole, fail to disclose, teach, or suggest a central processing unit adapted to process interrupt functions of *different priority levels*, one of said interrupt functions being processed ***upon receipt*** of a first interrupt request signal or a second interrupt request signal.

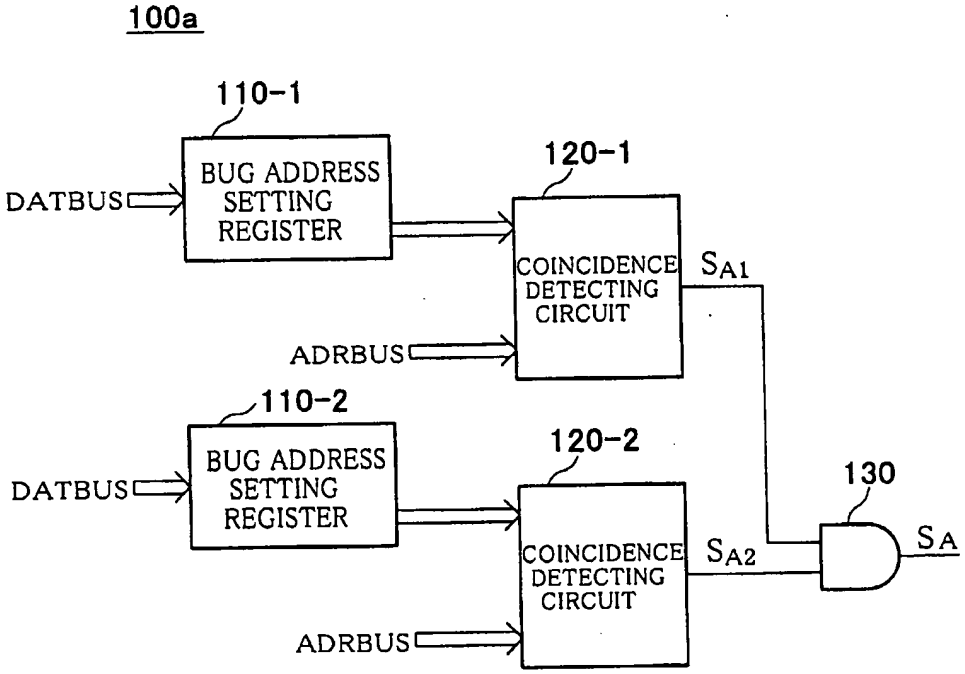
Sagane and Suzuki, either individually or as a whole, fail to disclose, teach, or suggest a counter register adapted to store a value, said value being *incremented by 1* when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address, wherein said counter register is *set to 0* during said initialization processing.

Withdrawal of this rejection is respectfully requested.

Claim 52 stands or falls alone - Claim 52 is drawn to a data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.

Figure 7 of the specification as originally filed is shown hereinbelow.

FIG.7



U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application, provides in paragraph [0073] that:

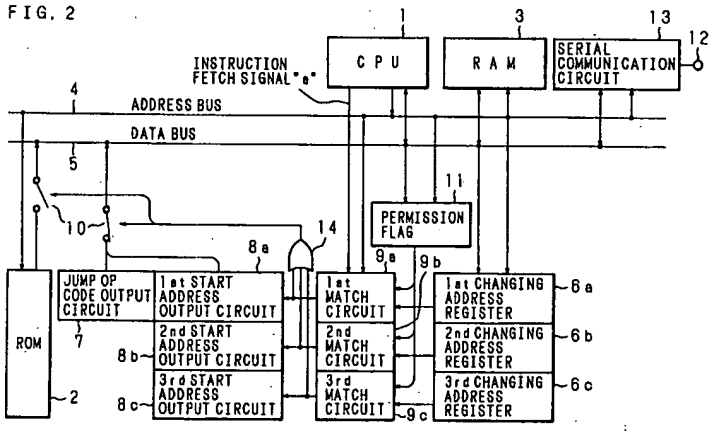
> [0073] When there is sufficient leeway in the interrupt processing of the CPU 10, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so a plurality of bug

processings have to be assigned to a single interruption. In this case, as shown in FIG. 7, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the output signal S_A Of the AND gate 130 is input to the CPU 10 as the interrupt request signal.

Sagane, Koscal and Suzuki - The Office Action admits that Sagane, Koscal and Suzuki do not expressly disclose that wherein said first and second interrupt request signals are input to said central processing unit as a single interruption (Office Action at page 18).

Hosotani - The Office Action cites Hosotani for the features that are admittedly absent from within Sagane, Koscal and Suzuki. Figure 2 of Hosotani is shown hereinbelow.

FIG. 2



Hosotani arguably teaches that *the CPU 1* is also connected, via the address bus 4 and a signal line of an instruction fetch signal a, to the *first to third match circuits 9a to 9c* that respectively compare the change addresses with the address on the address bus 4 in synchronism with the output timing of the instruction fetch signal a from *the CPU 1*, and output signals indicating the results of the comparisons (a "1" level indicates an address match, and a "0" level indicates an address mismatch) (Hosotani at column 4, lines 46-53).

However, Hosotani ***fails*** to disclose, teach, or suggest the signals from the first to third match circuits 9a-9c ***being input to CPU 1***.

The first to third match circuits 9a-9c are connected to a three-input OR circuit 14 (Hosotani at column 4, lines 60-61).

However, Hosotani ***fails*** to disclose, teach, or suggest the signals from the three-input OR circuit 14 ***being input to CPU 1***.

Instead, *the output of the OR circuit 14 is* ***connected to a connection control means 10*** which selects either the mask ROM 2 or a jump op code output circuit 7 and first to third start address output circuits 8a-8c for connection to the data bus 5 in accordance with the output level of the OR circuit 14 (which outputs a "1" level when the result of comparison from any one of the match circuits 9a-9c indicates a match, and a "0" level when all the comparison results indicate a mismatch) (Hosotani at column 4, line 61, to column 5, line 2).

- ***Thus, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.***

- ***Moreover, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are AND'ed together to become said single interruption.***

Withdrawal of this rejection is respectfully requested.

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

Dated: June 25, 2008

Respectfully submitted,

By _____ 40,290

Ronald P. Kananen
Registration No.: 24,104
Christopher M. Tobin
Registration No.: 40,290
RADER, FISHMAN & GRAUER PLLC
Correspondence Customer Number: 23353
Attorneys for Applicant

CLAIMS APPENDIX

1-26. (Canceled)

27. A data processing apparatus comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data;

a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal, said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address;

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

28. A data processing apparatus as set forth in claim 27, wherein said value is incremented when said interrupt request signal indicates said coincidence.

29-39. (Canceled)

40. A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address,

wherein another program address indicates a location within said program memory for another of the instruction codes, and

wherein said value of the counter register is incremented by 1.

41-44. (Canceled)

45. A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

46. A data processing apparatus as set forth in claim 45, wherein said counter register is located within a random access memory at a predetermined memory address.

47. A data processing apparatus as set forth in claim 45, further comprising:

bug address setting registers adapted to store said first and second bug addresses.

48. A data processing apparatus as set forth in claim 45, wherein said first bug address indicates a starting address within said program memory for a first buggy part of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program.

49. A data processing apparatus as set forth in claim 48, wherein said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part.

50. A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals.

51. A data processing apparatus as set forth in claim 45, wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.

52. A data processing apparatus as set forth in claim 51, wherein said first and second interrupt request signals are AND'ed together to become said single interruption.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

Within the Decision on Appeal mailed October 31, 2006, the Board of Patent Appeals and Interferences (the Board) concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of prior claims 13-25 under 35 U.S.C. §103.

Within the Decision on Rehearing mailed on June 21, 2007, the Board has maintained its earlier conclusion rendered in the Decision on Appeal of October 31, 2006 regarding claims 13-25.

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.